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(54) Method for protecting a stacked gate edge from self-aligned source (SAS) etch in a semiconductor device.

(57) A process for protecting the stacked gate edge of a semiconductor device is disclosed. The process provides for providing a spacer formation before the self aligned source (SAS) etch is accomplished. By providing the spacer formation prior to the SAS etch, tunnel oxide integrity is much improved and the source junction implant profile is much more uniform because the silicon around the source region is not gouged away.

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The present invention relates to semiconductor processing techniques and more particularly to self-aligned source (SAS) processing techniques.

In producing semiconductors and more particularly FLASH EPROM devices, the density of the device significantly enhances performance as well as cost effectiveness of the device. The typical way this increased density has been accomplished is through the use of a so-called self aligned source (SAS) etching technique which provides for the proper formation of the FLASH cell. An example of this type of technique is disclosed in U.S. Patent No. 5,120,671 entitled "PROCESS FOR SELF ALIGNING A SOURCE REGION WITH A FIELD OXIDE REGION AND A POLYSILICON GATE".

The above-identified patent discloses a method for forming a source region which is self-aligned with the poly word line as well as an apparatus formed thereby. In the patent, the end edges of the field oxide regions are vertically aligned with the poly word line with no bird's beak encroachment and corner rounding effect remaining in what will become the source region. The source region, formed between the ends of the field oxide regions of neighboring cells, is thus self-aligned with both the field oxide regions and the poly gate word lines. This self-alignment of the source region allows closer placement of poly word lines without any decrease in source width which thus requires less physical separation between (allows closer placement of) one memory cell to the next memory cell. Reduced cell size and greater overall device density is thus achieved.

In this example, the SAS etch is used after a stacked gate etch as a way to reduce overall cell size in a FLASH EPROM process. However, during the SAS etch, the stacked gate edge is exposed to the SAS etch, which has a significant negative impact on the tunnel oxide integrity. In addition, the building implants are done after the SAS etch. Since the SAS etch has a tendency to etch away or gouge away silicon under the source region, the implant profiles might not be uniform at the source and may change the profile of the surface source that overlaps below the stacked gate. In that case, the erase integrity distribution of the FLASH cell may be significantly degraded. As is well known, if the overlap area is too great source coupling may be higher than and interfere with the erase operation, and if it's too small, there may not be enough area for erasure.

Accordingly, what is needed is a system for ensuring that the overall cell size of semiconductor is reduced which doesn't have a negative impact on the tunnel oxide integrity of the device. In addition, the system should be one which the implant profiles are uniform at the source overlap region, thereby insuring cell integrity.

The present invention addresses such a need.

The present application discloses a method and system for protecting a stacked gate edge of a semiconductor device. The method comprises the step of providing the stacked gate edge on the semiconductor device, providing a spacer formation on the stacked gate edge and providing a self aligned source etch of the semiconductor device. In so doing, the stacked gate edge is protected thereby providing for tunnel oxide integrity and also providing for a more uniform source junction profile than those provided by previously known processes.

The method and system have particular application in a FLASH EPROM cell technology. With the described method and system the increased cell density associated with the FLASH cell is maintained, while the above-mentioned problems with tunnel oxide integrity and source junction profile are eliminated.

In the accompanying drawings, by way of example:

Figure 1 is a top view of a portion of a memory device.

Figures 2-4 are side views of the memory device of Figure 1.

Figure 4a is a sectional view of the memory device of Figure 1.

Figure 5 is a cutaway perspective view of the source side view of a conventional FLASH cell after the SAS etch showing the source profile provided if source implant is after self aligned source (SAS) etch in the prior art.

Figures 6-10 are cutaway perspective views of a FLASH cell as it proceeds through a conventional (prior art) process.

Figure 11 is a simple flow chart of the process of providing a FLASH cell in accordance with the present invention.

Figure 12 is a detailed flow chart of the process of Figure 11.

Figure 13 is a cutaway view of the FLASH cell before the SAS etch in accordance with the process flow of the present invention.

Figure 14 is a cutaway view of the FLASH cell after the SAS etch.

The present invention is related to an improvement in the processing of a semiconductor circuit, particularly a FLASH EPROM cell. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment will be readily apparent to those skilled in the art and the generic principles herein may be applied to other embodiments. Thus, the present invention is not intended to be limited to the embodiment shown but is to be accorded the widest scope consistent with the prin-

ciples and features described herein.

With reference to the drawings, Figure 1 illustrates a top view of a portion of a memory device formed in accordance with a conventional process. In this process, field oxide regions 31 and 33 are formed by growing oxide between parallel rows of nitride regions 18 to form the field oxide regions 31 and 33 as continuous lines across the source line 12 formed in the openings of a latticework of nitride regions 18. A layer of polysilicon is then deposited over the field oxide regions 31 and 33. After placing a photoresist mask over the polysilicon, the portions of the polysilicon left exposed are etched away. The remaining portions of polysilicon are poly word lines 9 and 11, which run parallel to source line 12.

Etching the polysilicon to form poly word lines 9 and 11 exposes the underlying field oxide regions 31 and 33 in the region of source line 12. Source mask 41 is then placed over the memory device and the oxide regions 31 and 33 are then etched away where they were exposed by the etching of poly word lines 9 and 11. This field oxide etch, which uses a high selectivity etch, as is discussed in more detail below, reduces field oxide regions 31 and 33 into separate field oxide regions 13, 15, 17 and 19. More importantly, this field oxide etch aligns field oxide regions 13 and 15, as well as 17 and 19, with the edges of poly word lines 9 and 11. Thus, when source implantation occurs it is self-aligned to the coincident edges of the field oxide and the polysilicon regions.

It is important to note that the source mask 41 is not used to align the source region implantation with the edges of the poly word lines. The source mask 41 is placed on the memory device to protect (during implantation) the portions of the field oxide regions 31 and 33 which reside on the other side of the poly word lines 9 and 11 from the source region 12 and between which the drain regions 14 will later be formed.

The formation and resulting alignment of field oxide regions 17 and 19 with poly word lines 9 and 11 is further shown in side views in Figures 2-4. Referring now to Figure 2, field oxide 33 is formed on the silicon substrate 29. Polysilicon 35 is then deposited on the field oxide 33. A photoresist mask 39 is then placed on top of the polysilicon 35 leaving select portions of the polysilicon exposed. Note that a direct write technique, using for example an electron beam or a laser beam, could also be used to create the mask pattern in the photoresist.

Etching the exposed polysilicon 35 through the photoresist mask 39 of Figure 2 yields the formation, as shown in Figure 3, where the only remaining polysilicon is that which was protected by the opaque portions of photoresist mask 39. The remaining polysilicon portions are poly word lines 9 and 11. Note that Figure 2 represents a cross-sectional view of Figure 1 along line a-a and shows the continuous field oxide layer 33 underlying poly word lines 9 and 11.

Having formed poly word lines 9 and 11, by etching the exposed polysilicon through the mask 39, exposes portions of the underlying field oxide 33. In the preferred embodiment, mask 41 is then placed on the device to protect the drain regions and then the field oxide portions are etched away using a high selectivity oxide etch, as is discussed more fully below. Referring now to Figure 4, after etching field oxide 33, the portions that remain are field oxide regions 17 and 19.

Referring to Figure 4A, what is shown is the cross section of the active cell region at the same point in the process.

Referring now to Figure 5, what is shown is an enlarged cutaway diagram of a FLASH EPROM cell 100 which has been processed in accordance with the prior art. This cell 100 comprises first and second polysilicon layers 102 and 103 and oxide region 104 therebetween, and a tunnel oxide region 106 between the first poly silicon layer 102 and the silicon area 108. In such a cell, the SAS etch 110 could effect the tunnel oxide region 106 and also could cause gouging of the implant regions 112 and 114.

To more specifically describe how this might occur, refer now to Figures 6 through 10, which show the various stages of the operation of the prior art process. Referring to Figure 6, initially a stacked gate etch is applied to the polysilicon region 102. Then, thereafter, referring to Figure 7, an SAS mask 202 is placed on top of the device to allow for certain portions of the oxide to be masked. Thereafter there is an SAS etch 204 which essentially removes a portion of the silicon area shown in Figure 8. In Figure 9, a first implant is provided, and a resist strip is applied, as is seen this implant could be brought to a position well inside the gate area of the device. The second implant is provided to provide the drain region shown in Figure 10. As is seen in Figure 10, the resultant cell could have significant tunnel oxide erosion as well as degraded silicon doping due to silicon gouge from the SAS etch process.

The present invention addresses these problems by using a spacer formation to protect the stacked gate edge from exposure to the SAS process. Since this spacer formation is already inherent in nearly all CMOS processes as described above with reference to Figures 1-4, existing process techniques do not have to be made significantly more complicated to provide the spacing. Through the use of this spacer formation, the SAS does not affect the doped areas nor does it affect

the tunnel oxide region.

To more specifically describe the features of the present invention, refer now to Figure 11, which is a simple flow chart showing the process in accordance with the present invention. Accordingly this process comprises providing a stacked gate edge, via step 302. The spacer formation is then provided, via step 304. Thereafter, the source aligned gate etch is provided, via step 306.

To describe this process with reference to a preferred embodiment refer now to Figure 12 which shows a detailed flow chart of the process shown in Figure 11. Referring now to Figure 12, what is shown is a flow chart of the method for protecting the tunnel oxide, stacked gate edge and source junction function profile of a device. First, the stacked gate etch takes place, via step 402. Then the resist strip takes place, via step 404. Next a thin oxide or oxidation for implant screen is provided to protect the tunnel oxide region, via step 406.

Thereafter, the double diffused implant (DDI) mask and DDI implant takes place, via step 408 and another resist strip takes place, via step 410. Thereafter the modified drain diffusion (MDD) mask and implant takes place via step 412 and another resist strip takes place, via step 413. Thereafter a N-lightly doped drain (LDD) mask and implant and a P-LDD implant mask and implant is provided, via steps 415 and 416 and a antipunch through (AT) implant is provided, via step 418.

Then the spacer deposition is provided via step 420. Finally, the spacer is etched, via step 422. At this point, the cross section of the core cell 500 looks like that shown in Figure 12. Accordingly, the stacked gate edge 502 is protected by the spacer formation 504. Thereafter the process for providing SAS process etch can then occur. Referring back to Figure 13, an SAS mask is provided, via step 424. Then the SAS etch can be provided, via step 426. Thereafter the spacer formation oxidation takes place, via step 428. Then the N+ S/D mask and DDI mask (a critical mask) are provided, via step 430. Finally, the N+ source/drain (S/D) implant and a source implant are provided via step 432. The implant step 432 is used to connect the source line from the actual source region and field region that is SAS etched. The cross section of the resulting cell 500 will look like that shown in Figure 14. In this cell the tunnel oxide integrity is improved and there is a uniform source region due to the spacer formation 504. Therefore, the source implant is not provided to a gouged portion of the silicon. Accordingly, a uniform source region is provided under the gate.

Accordingly, by providing the spacer formation prior to the SAS etch the tunnel oxide region integrity is much improved in addition through the use of the process of the present invention stacked gate edge is immune to gouging and as well as allowing for an improved source junction profile.

It should be understood that although the present invention has been described in conjunction with a specific type of cell (FLASH EPROM) it should be recognized by one of ordinary skill in the art that many types of cells can be produced utilizing this process. It should also be recognized that many types of materials and processes can be utilized to provide the resist strip, etch, and implants and they would be within the spirit and scope of the present invention.

Although the present invention has been described in accordance with the embodiments shown in the figures one of ordinary skill in the art will recognize there could be variations to those embodiments and such variations may be within the scope of the present invention. Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the scope of the present invention, the scope of which is defined by the appended claims.

Claims

1. A method for protecting a stacked gate edge to minimize damage to a tunnel oxide and to maintain source junction uniformity of a semiconductor device comprising the steps of:
   (a) providing the stacked gate edge on the semiconductor device;
   (b) providing a spacer formation on the stacked gate edge; and
   (c) providing a self aligned source (SAS) on the semiconductor device.

2. The method of claim 1 in which the stacked gate edge providing step (a) further comprises the step of:
   etching the stacked gate edge.

3. The method of claim 2 in which the stacked gate edge providing step (a) further comprises the step of:
   providing a resist strip;
   providing an oxidation layer; and
   providing a mask and an implant on the semiconductor device.

4. The method of claim 1 in which the spacer formation step (b) further comprises the steps of:
   depositing a spacer material; and
   etching the spacer material to form the spacer formation.

5. The method of claim 1 in which the SAS providing step (c) further comprises the steps of:

providing an SAS mask; and

etching the SAS mask.

6. The method of claim 5 in which the SAS providing step (c) further comprises the steps of:

providing an oxidation layer on the spacer formation;

masking the semiconductor device; and

implanting a material to connect source line from a source region to a field region of the semiconductor device.

7. A system for protecting a stacked gate edge to minimize damage to a tunnel oxide region and to maintain source junction uniformity of a semiconductor device comprising:

means for providing the stacked gate edge on the semiconductor device;

means responsive to the stacked gate edge providing means for providing a spacer formation on the stacked gate edge; and

means responsive to the spacer formation providing means for providing a self aligned source (SAS) on the semiconductor device.

8. The system of claim 7 in which the stacked gate edge providing means further comprises:

means for etching the stacked gate edge.

9. The system of claim 8 in which the stacked gate edge providing means further comprises:

means for providing a resist strip;

means responsive to resist strip providing means for providing an oxidation layer; and

means responsive to the oxidation layer providing means for providing a mask and implant on the semiconductor device.

10. The system of claim 7 in which the spacer formation means further comprises:

means for depositing a spacer material; and

means responsive to the depositing means for etching the spacer material to form the spacer formation.

11. The system of claim 7 in which the SAS providing means further comprises:

means for providing an SAS mask; and

means responsive to the SAS mask providing means for etching the SAS mask.

12. The system of claim 11 in which the SAS providing means further comprises:

means for providing an oxidation layer on the spacer formation;

means responsive to the oxidation layer providing means for masking the semiconductor device; and

means responsive to the masking means for implanting a material to connect source line from a source region to a field region of the semiconductor device.

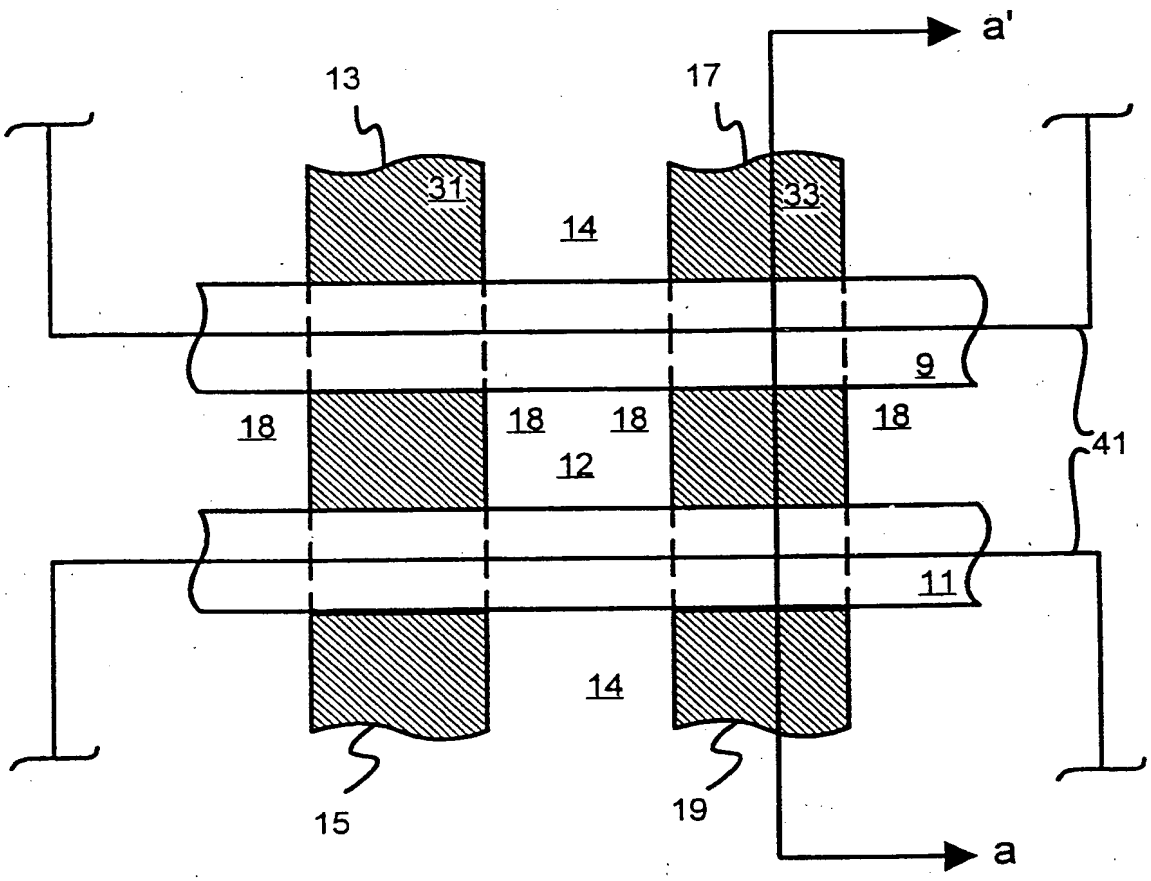
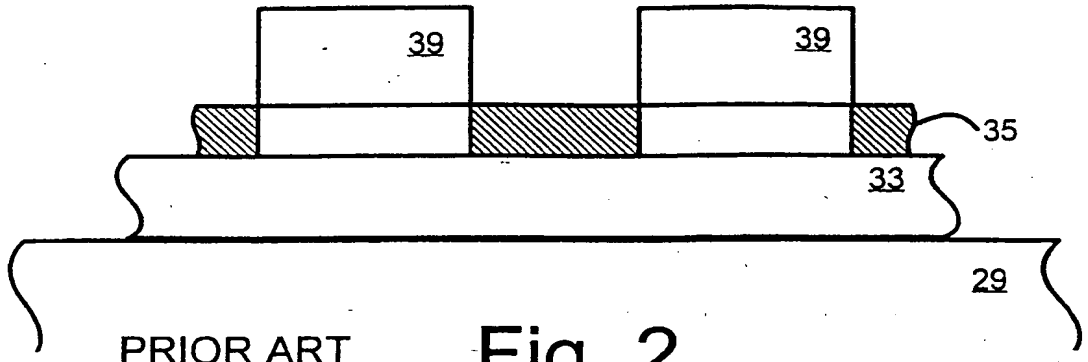


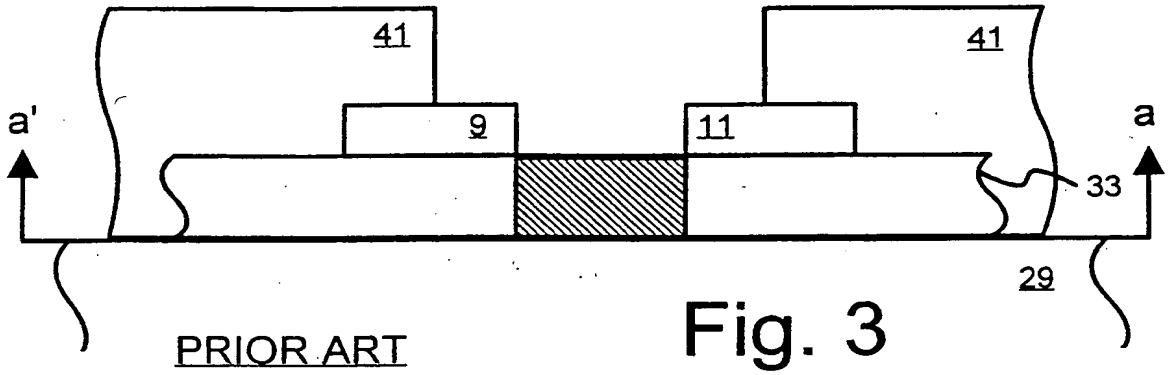
Fig. 1

PRIOR ART



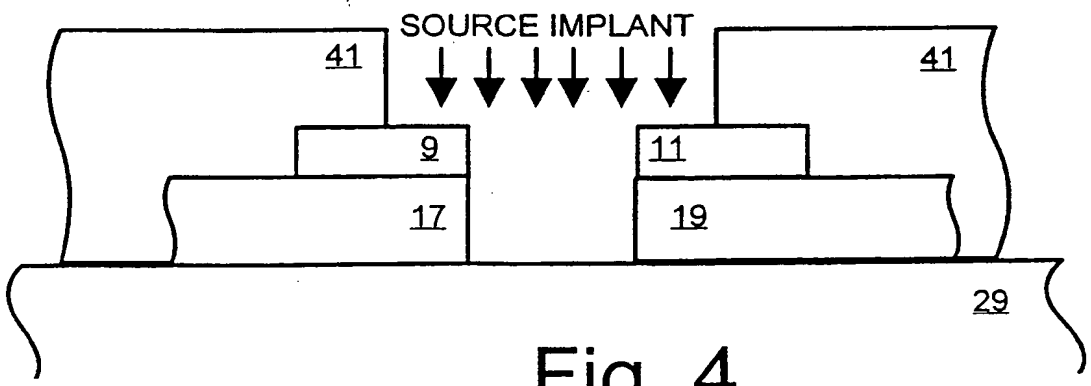
PRIOR ART

Fig. 2



PRIOR ART

Fig. 3



PRIOR ART

Fig. 4

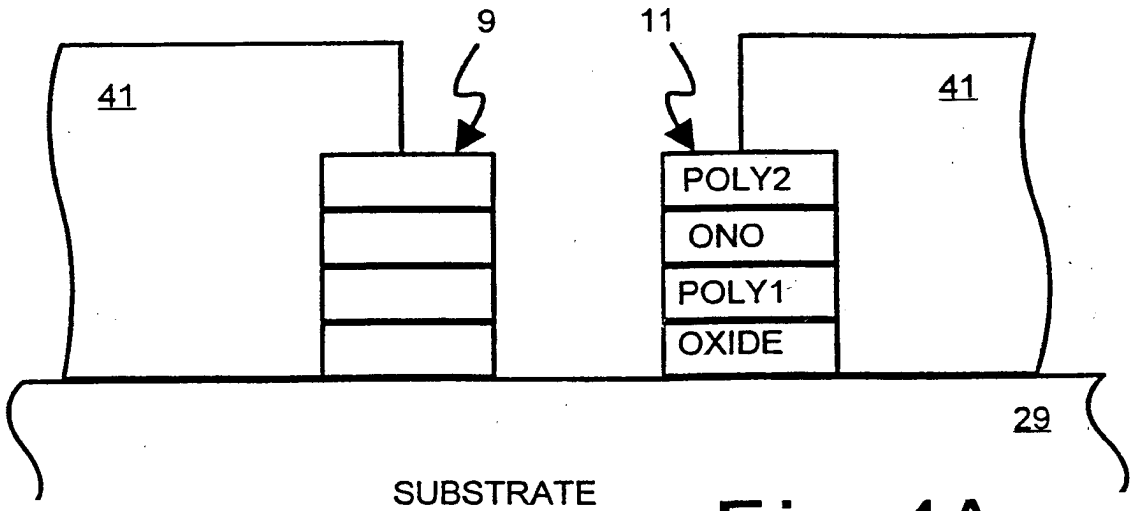

9
11
41
41
POLY2
ONO
POLY1
OXIDE
29
SUBSTRATE

Fig. 4A

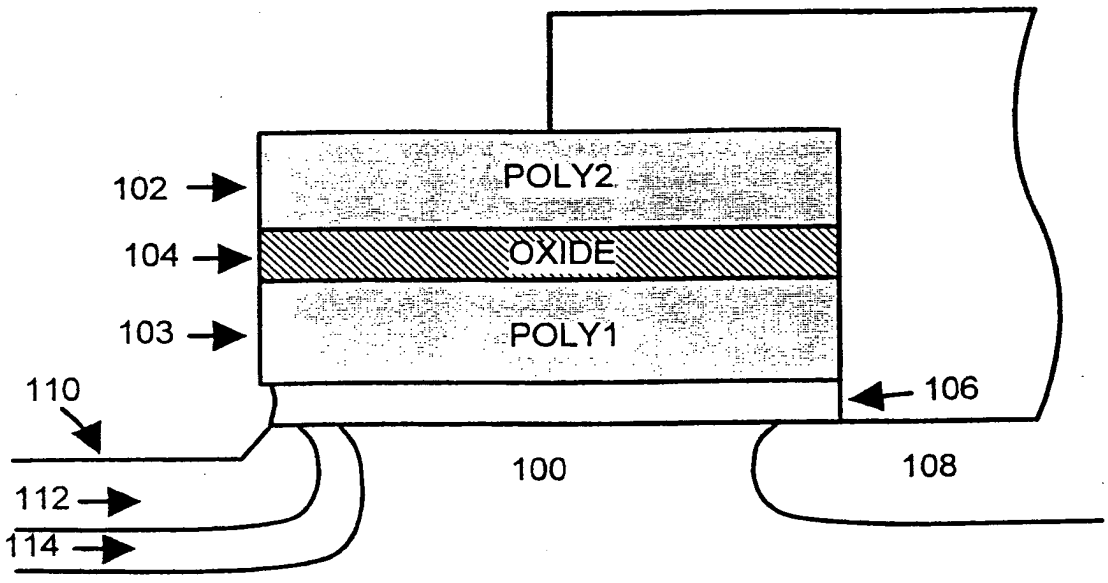

102
104
103
110
112
114
POLY2
OXIDE
POLY1
106
100
108

Fig. 5

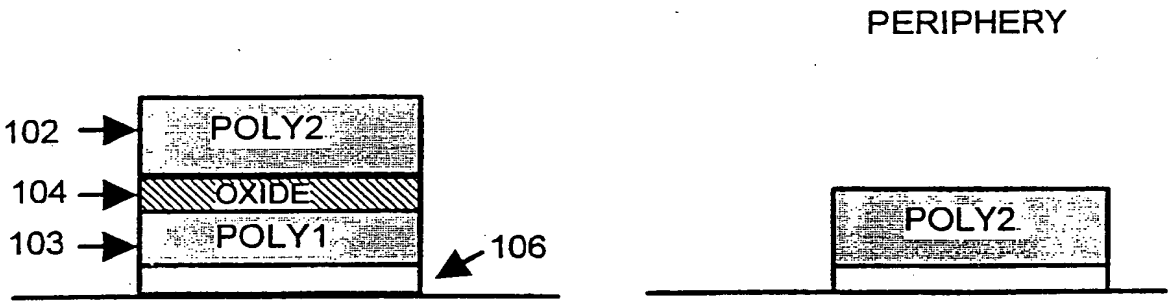

PERIPHERY
102
104
103
POLY2
OXIDE
POLY1
106
POLY2

Fig. 6

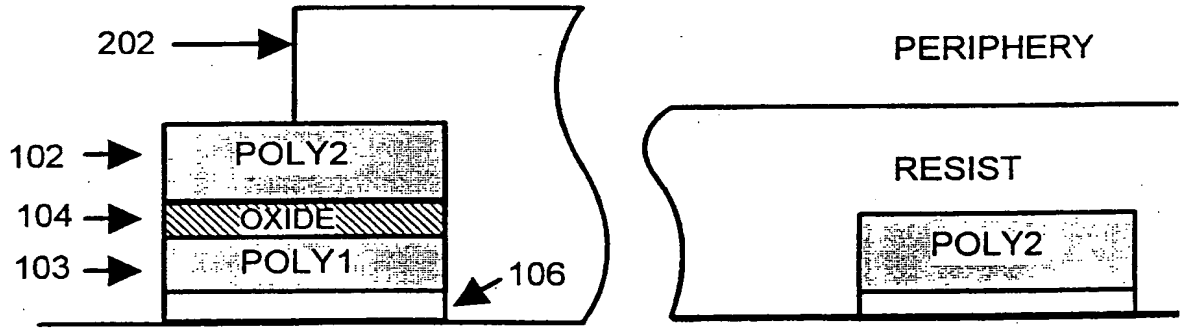

202
PERIPHERY
102
104
103
POLY2
OXIDE
POLY1
106
RESIST
POLY2

Fig. 7

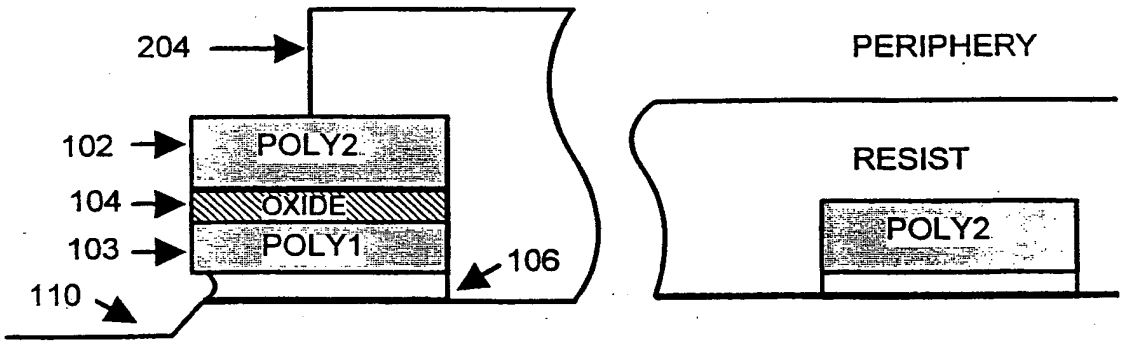

204
102
104
103
110
POLY2
OXIDE
POLY1
106
PERIPHERY
RESIST
POLY2

Fig. 8

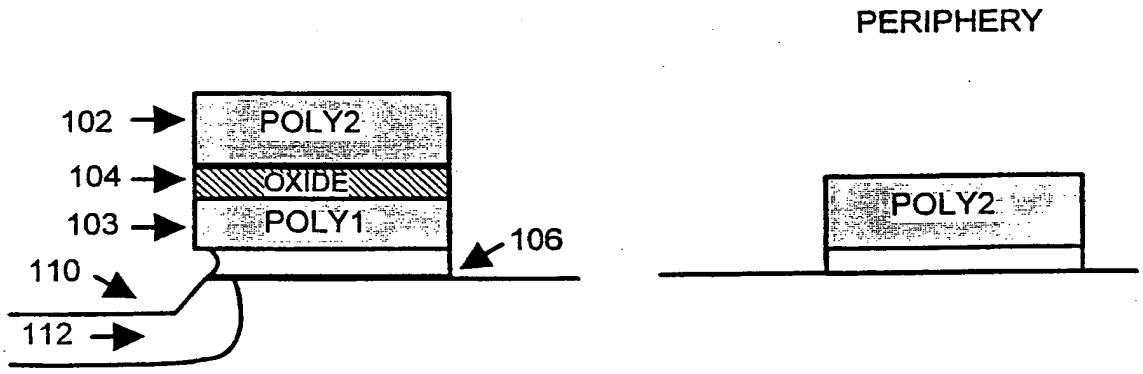

PERIPHERY
102
104
103
110
112
POLY2
OXIDE
POLY1
106
POLY2

Fig. 9

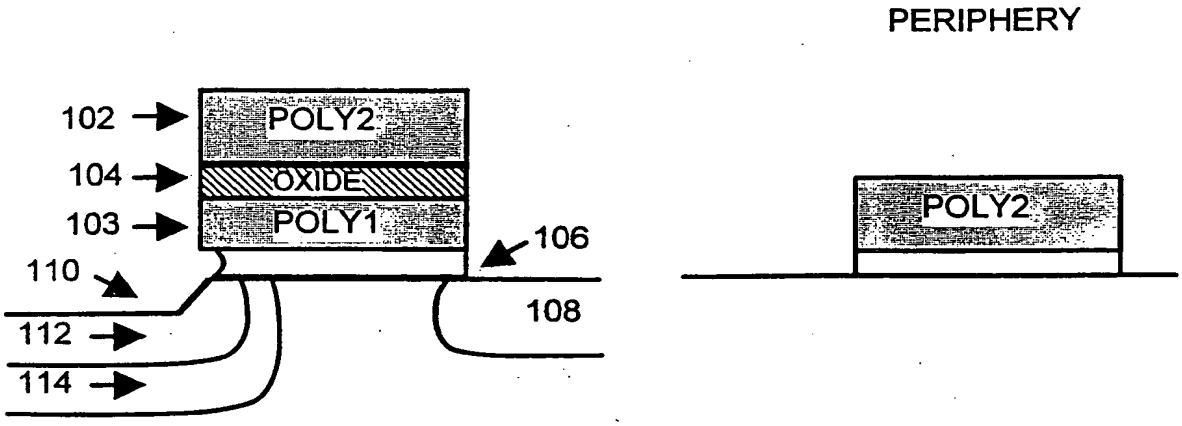


Fig. 10

Fig. 12

Fig. 12A

Fig. 12B

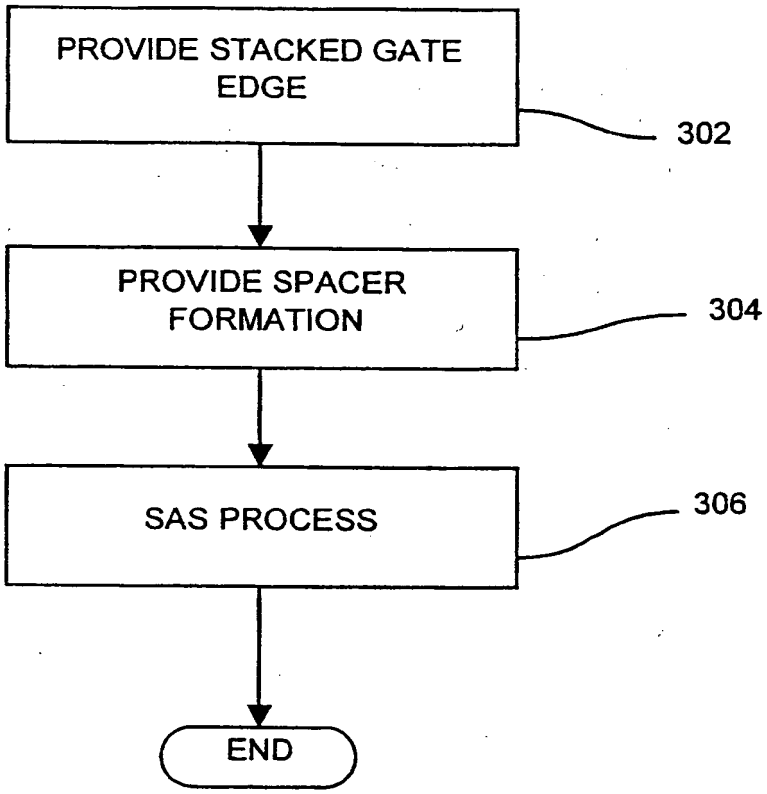

PROVIDE STACKED GATE EDGE
302
PROVIDE SPACER FORMATION
304
SAS PROCESS
306
END

Fig. 11

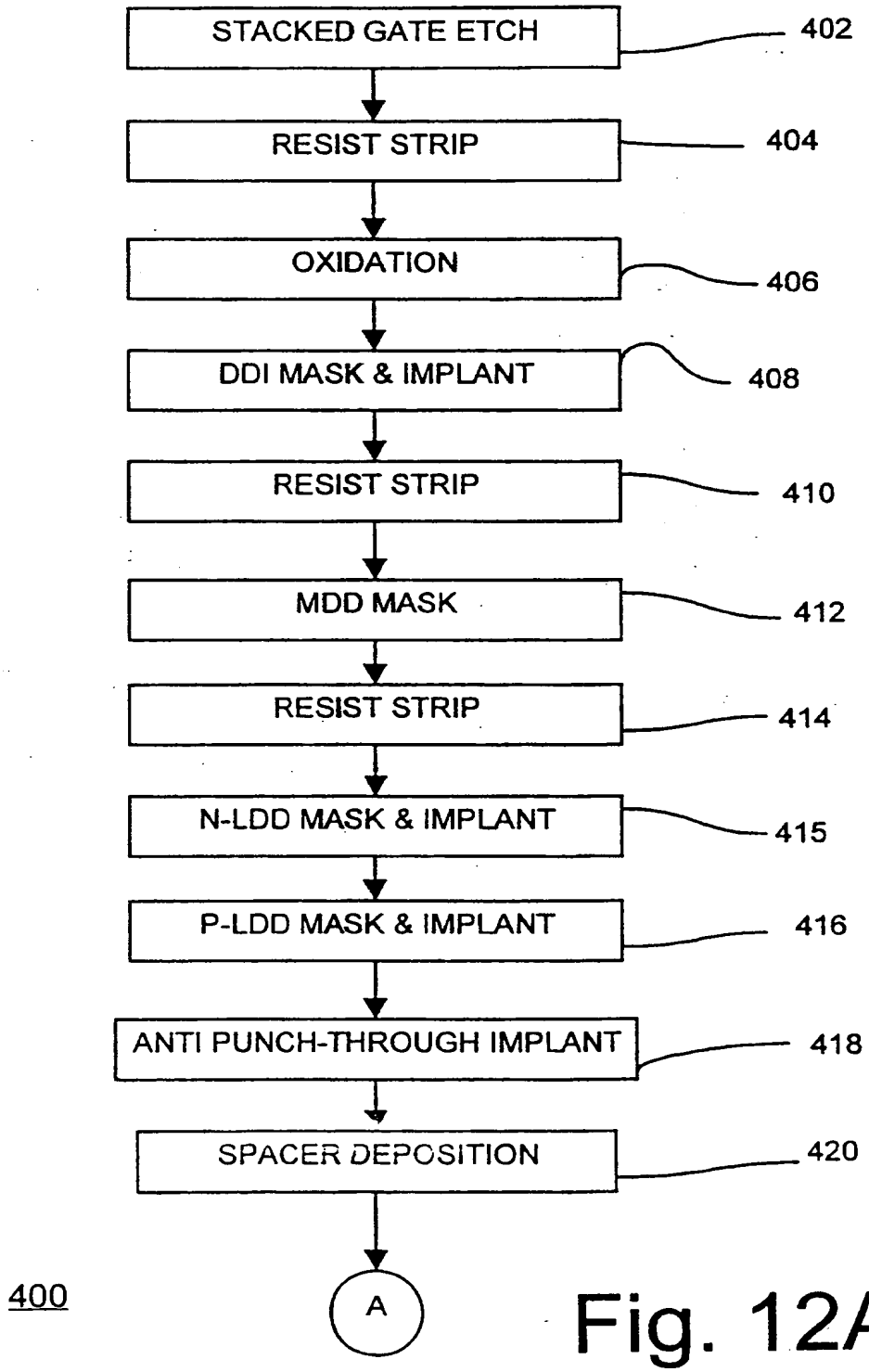
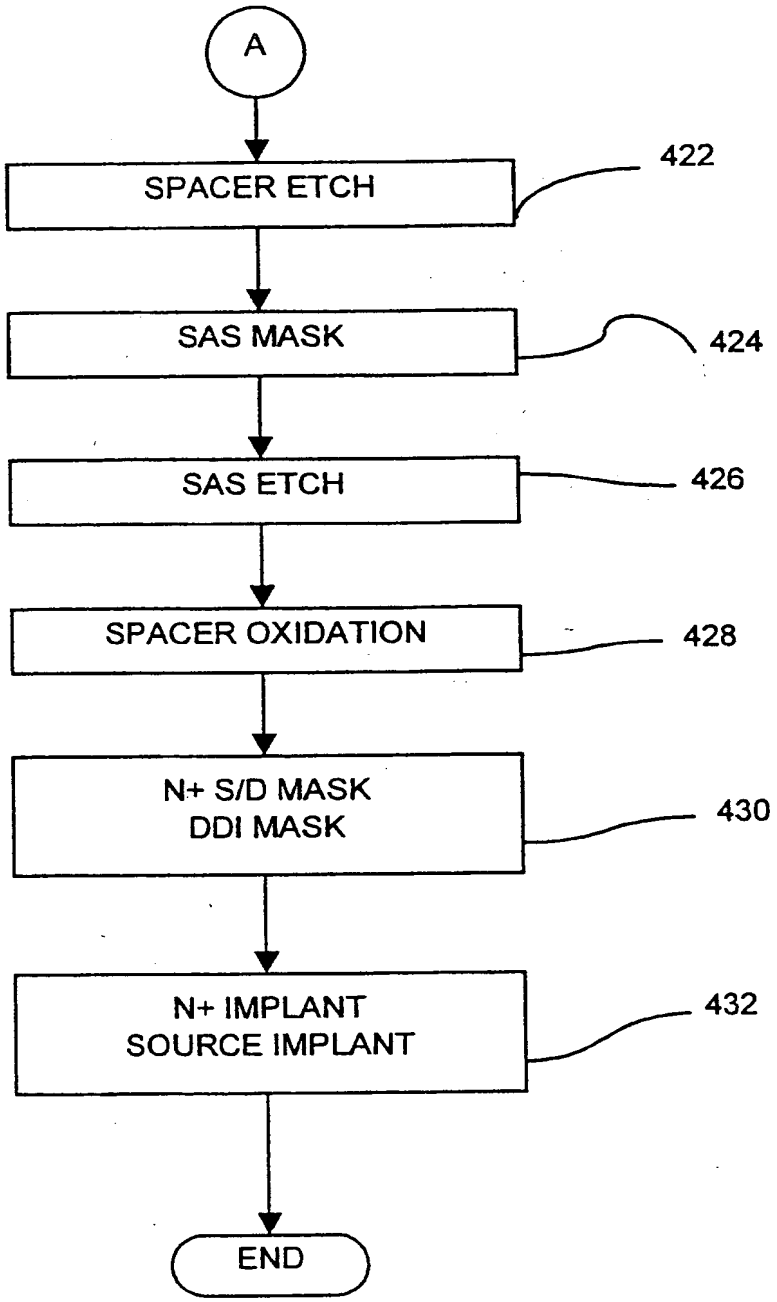

STACKED GATE ETCH
402
RESIST STRIP
404
OXIDATION
406
DDI MASK & IMPLANT
408
RESIST STRIP
410
MDD MASK
412
RESIST STRIP
414
N-LDD MASK & IMPLANT
415
P-LDD MASK & IMPLANT
416
ANTI PUNCH-THROUGH IMPLANT
418
SPACER DEPOSITION
420
A
400

Fig. 12A


A
SPACER ETCH
422
SAS MASK
424
SAS ETCH
426
SPACER OXIDATION
428
N+ S/D MASK
DDI MASK
430
N+ IMPLANT
SOURCE IMPLANT
432
END

400

Fig. 12B

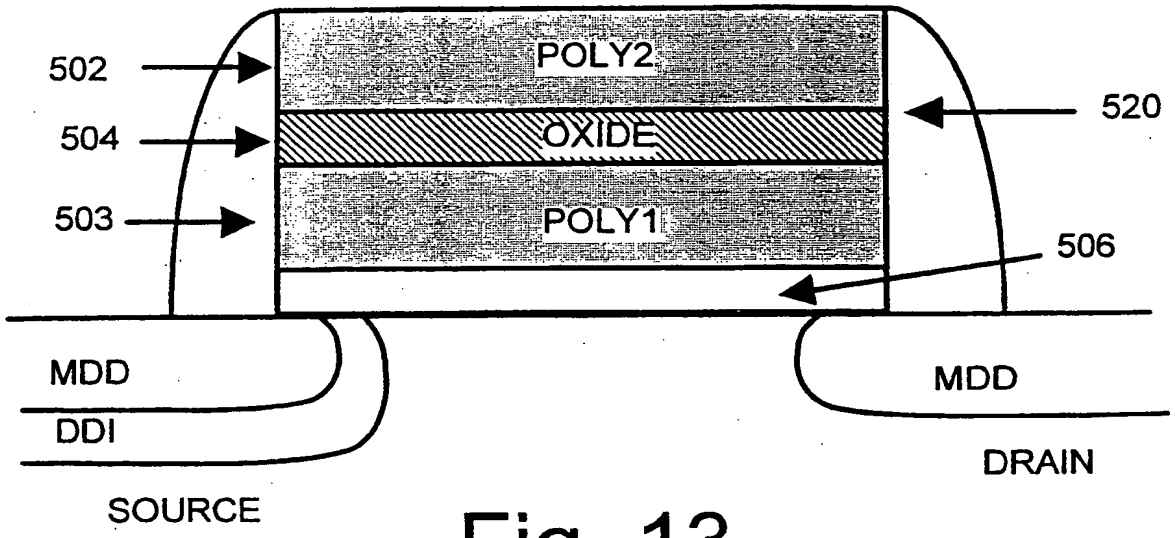

502
504
503
POLY2
OXIDE
POLY1
520
506
MDD
DDI
SOURCE
MDD
DRAIN

Fig. 13

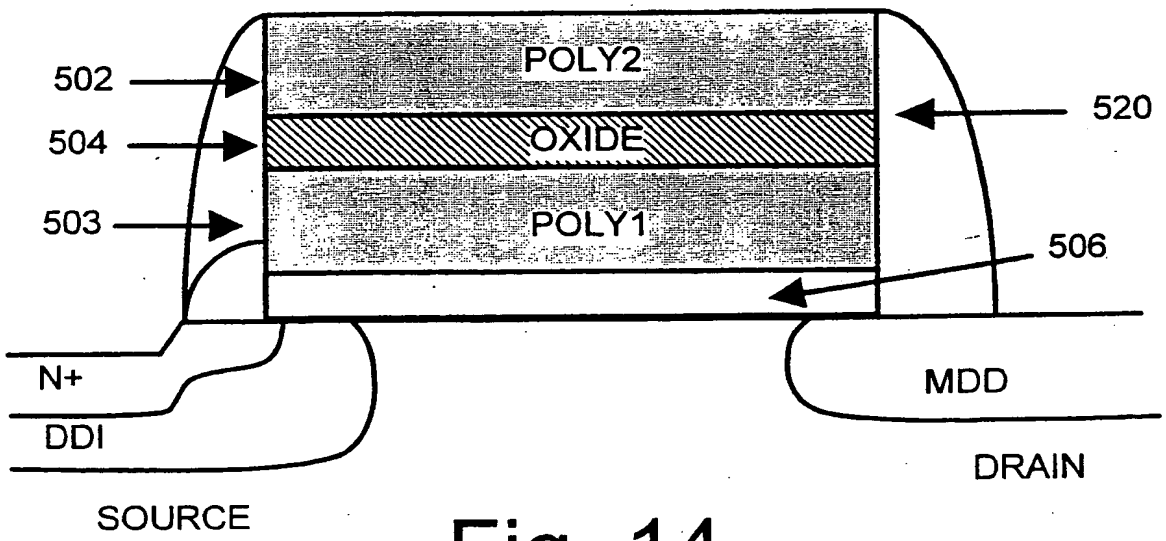

502
504
503
POLY2
OXIDE
POLY1
520
506
N+
DDI
SOURCE
MDD
DRAIN

Fig. 14

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(54) Method for protecting a stacked gate edge from self-aligned source (SAS) etch in a semiconductor device

(57) A process for protecting the stacked gate edge of a semiconductor device is disclosed. The process provides for providing a spacer formation before the self aligned source (SAS) etch is accomplished. By providing the spacer formation prior to the SAS etch, tunnel oxide integrity is much improved and the source junction implant profile is much more uniform because the silicon around the source region is not gouged away.

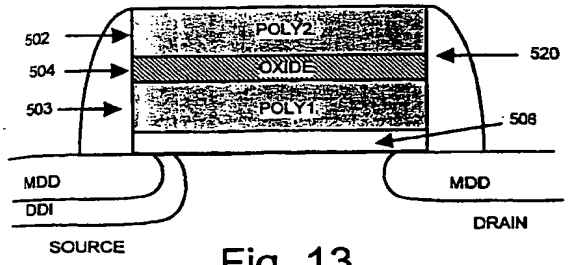

Fig. 13

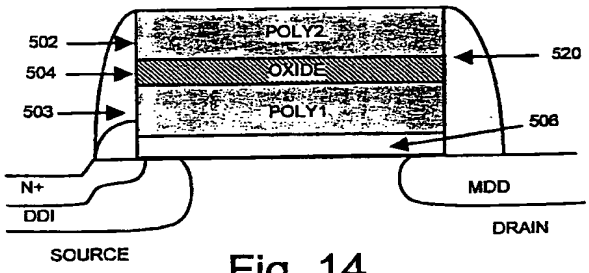

Fig. 14

EP 0 680 080 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 95 30 1952

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	US 5 149 665 A (LEE RUOJIA) 22 September 1992 * column 1, line 7 - line 33 * * column 1, line 61 - column 2, line 45; figures 1,2 * * column 4, line 1 - line 30 * * column 5, line 55 - column 6, line 67; figures 9-17 * * column 7, line 4 - line 9 *	1,2,4-8, 10-12	H01L21/8247 H01L21/336 H01L21/28 H01L27/115
Y		3,9	
Y	US 5 175 120 A (LEE ROGER R) 29 December 1992 * column 1, line 10 - line 15 * * column 5, line 50 - column 6, line 59; figures 7-11 *	3,9	
A		1,2,4,7, 8,10	
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	29 October 1997	Klopfenstein, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
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EUROPEAN SEARCH REPORT

Application Number
EP 95 30 1952

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	EP 0 412 558 A (TOKYO SHIBAURA ELECTRIC CO) 13 February 1991 * column 1, line 1 - column 2, line 10; figure 1 * * column 5, line 30 - column 6, line 33; figures 3A-3D,4A-4C * * figures 5A-5C * * column 10, line 1 - line 52; figures 8A-8F,9A-9F * * column 11, line 32 - line 49 * * column 12, line 12 - line 17 * * column 12, line 25 - line 33 *	1,2,4,5, 7,8,10, 11	
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X	PATENT ABSTRACTS OF JAPAN vol. 018, no. 174 (E-1530), 24 March 1994 & JP 05 343693 A (TOSHIBA CORP), 24 December 1993, * abstract *	1,2,4,5, 7,8,10, 11	
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Application Number
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A	US 5 087 584 A (WADA GLEN N ET AL) 11 February 1992 * column 4, line 5 - column 7, line 24; figures 1-8 * -----	1-12	

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
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